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AN052

AOS Drive Electronics Latency Measurements

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1 Introduction

This application note describes results of testing establishing elements of the latency of the current AOS Drive Electronics. Figure 1 shows the basic internal architecture of the drive electronics. The user sends either an LVDS signal or an Ethernet signal into the drive electronics to command voltages. This signal is clocked into an FPGA that conditions commands to a series of digital to analog converters (DACs). Each low-voltage DAC signal (LV1) is then sent through a high voltage amplifier before being transmitted through a 37D subminiature connector to an actuator. In this application note, we will be testing the transmission time at a variety of these points.

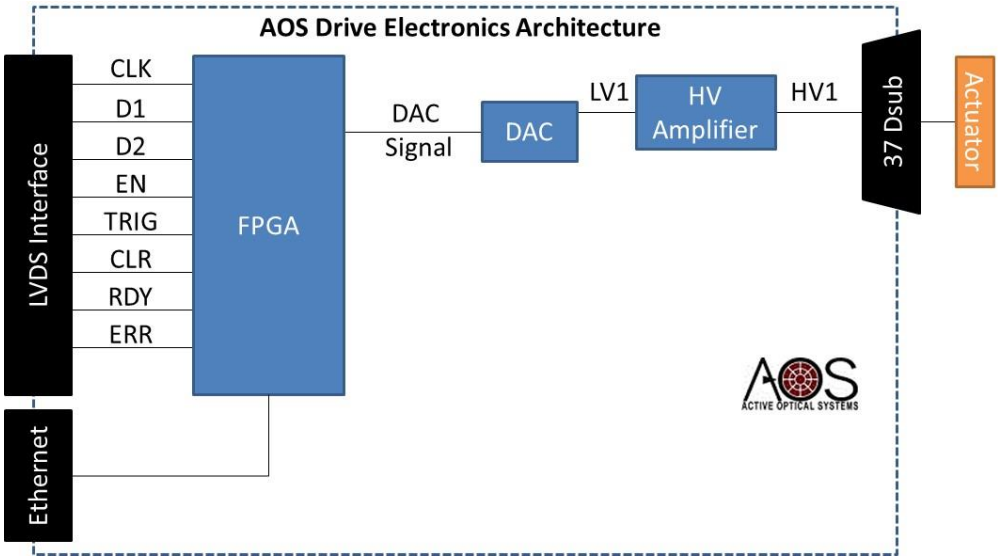

Figure 1: Drive Electronics Architecture

2 Approach and Results

Given the electronic layers available in this drive electronics architecture, we have a variety of locations in which we can sample the progression of a signal from the LVDS digital interface to the 37 D-sub analog high voltage output. We began our measurements by examining the chip select signal going to the DAC from the

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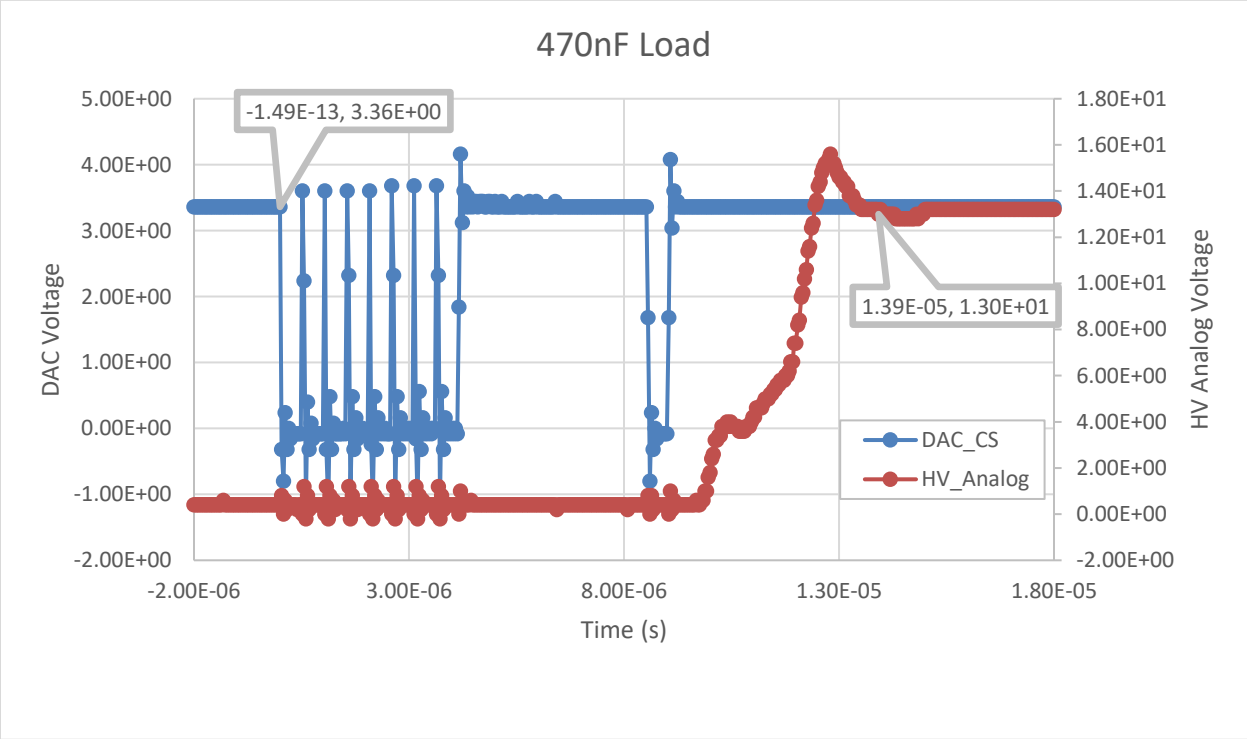
FPGA and the analog high voltage output signal while driving a 470nF ceramic capacitor, which is more than a factor of two larger than our standard actuator load. For this experiment, we used the Ethernet command interface, but expect no difference in these measurements while using the LVDS interface. We then examined the latency between the first LVDS bit into the system to convergence of the analog output.

2.1 DAC to Analog Output Latency

Figure 2 shows the results of these measurements from an oscilloscope. The oscilloscope was set to trigger on the falling edge of the chip select (CS) signal, so the time axis starts on this edge. The DAC has 8-channels, so the CS signal is first seen here bounding each 16-bit write. Then there is a pause between the last digital write and the final command that triggers the DAC write to allow the FPGA time to process the inter-actuator limit checking. After the final trigger command we almost immediately see the analog voltage begin to change. The time to convergence of the high voltage analog output with the capacitive load is about 14µs and 12µs for the rise and fall times respectively. The time between the first DAC command out to the last DAC command (digital write latency) is about 9µs.



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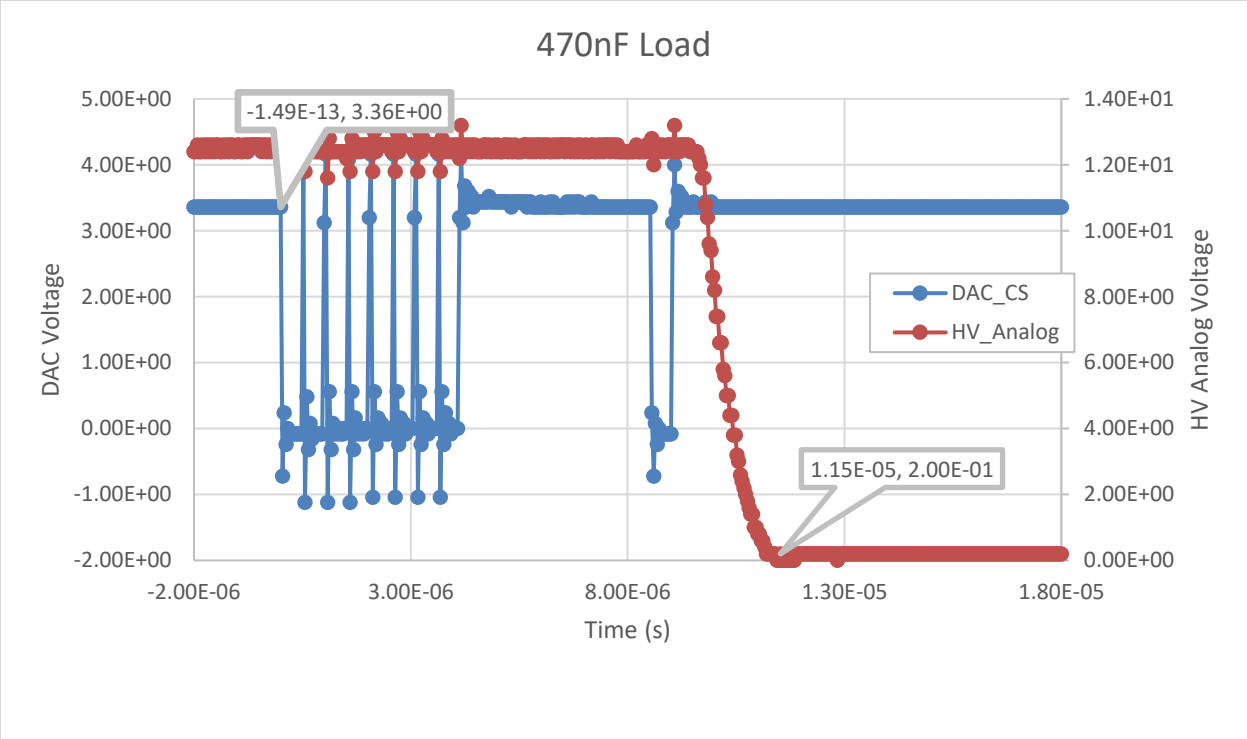

Figure 2: (top) Rise Time; (bottom) Fall Time

2.2 Total System Latency

We then examined the total system latency using the LVDS interface. For this test we probed the LVDS enable line and the analog output line, which was again loaded with the 470nF capacitor. For this testing we did a 30V (25% range) step. Figure 5 shows the results of this testing. The time between the first bit out of the LVDS interface to convergence of the high voltage analog signal in rise and fall were both less than 28 µs.

2.3 Larger Capacitor Latency

Larger capacitors will have additional analog latency associated with the current limitation of the standard drive electronics amplifiers. Figure 3 and Figure 4 show the analog rise and fall times for the 3.3µF and 10µF loads. For this section, we use a 10% to 90% rise and fall time definition. For a 64V step, the 3.3µF capacitor had a 4.2ms fall time and 2.6ms rise time. For a full 120V step, this corresponds to approximately a 8ms fall and 5ms rise time. For a 32V step, the 10µF capacitor had a 4ms fall time and a 2.4ms rise time. Scaling to a 120V step, we expect this to be a 16ms fall and 9ms rise time.

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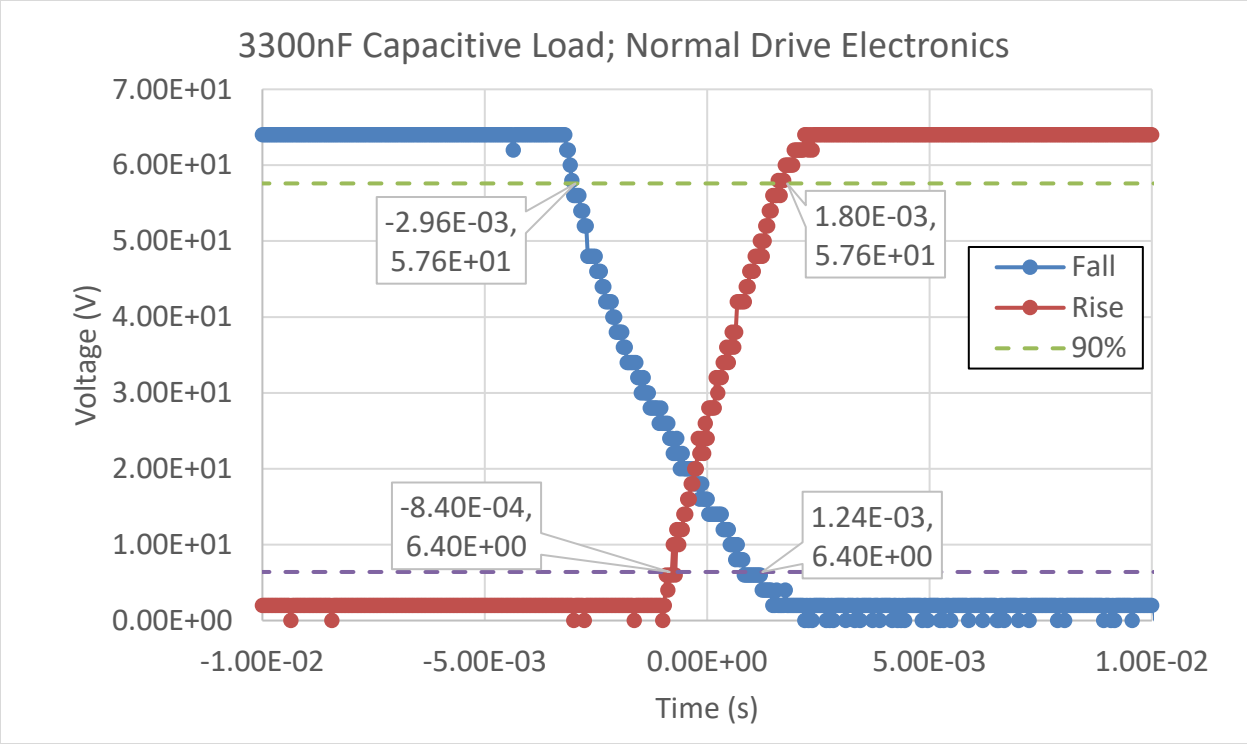

Figure 3: Analog Rise and Fall Times of a 3300nF Capacitive Load

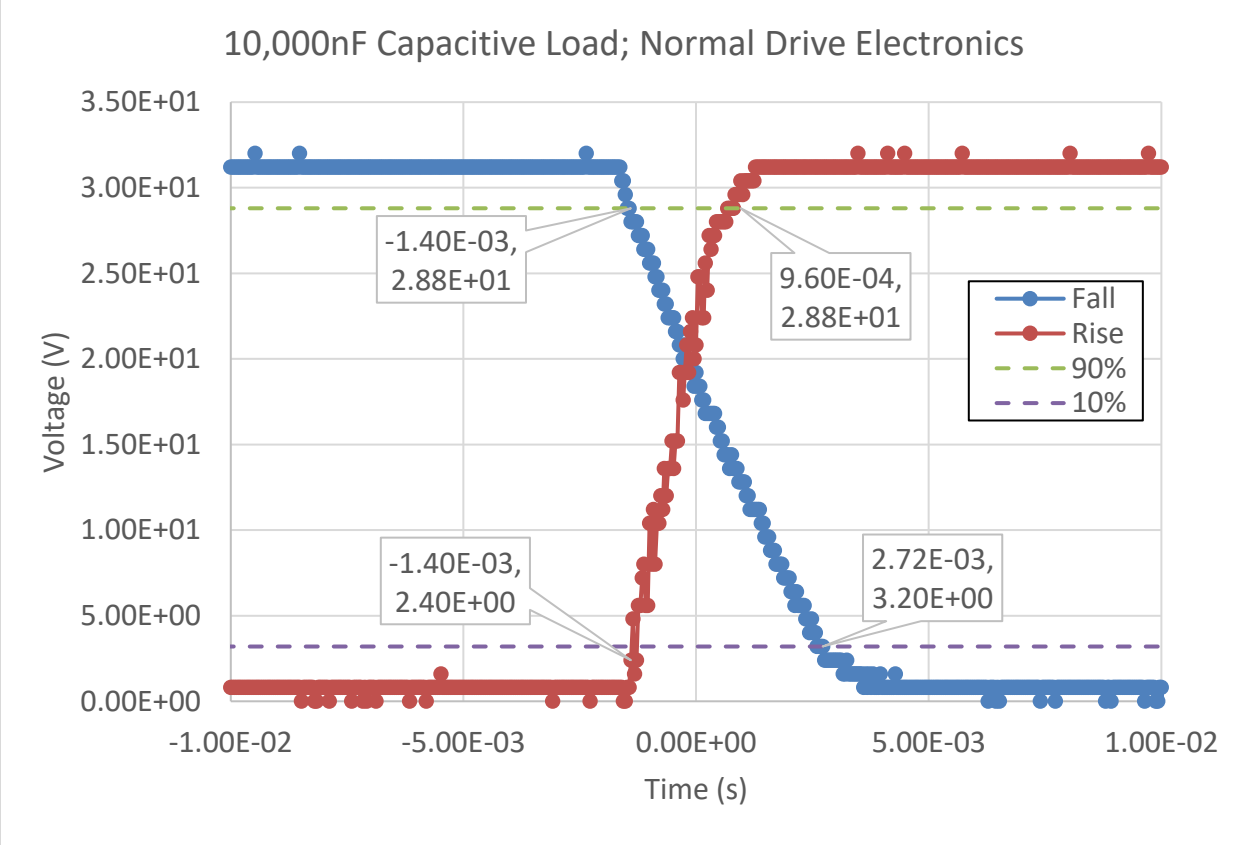

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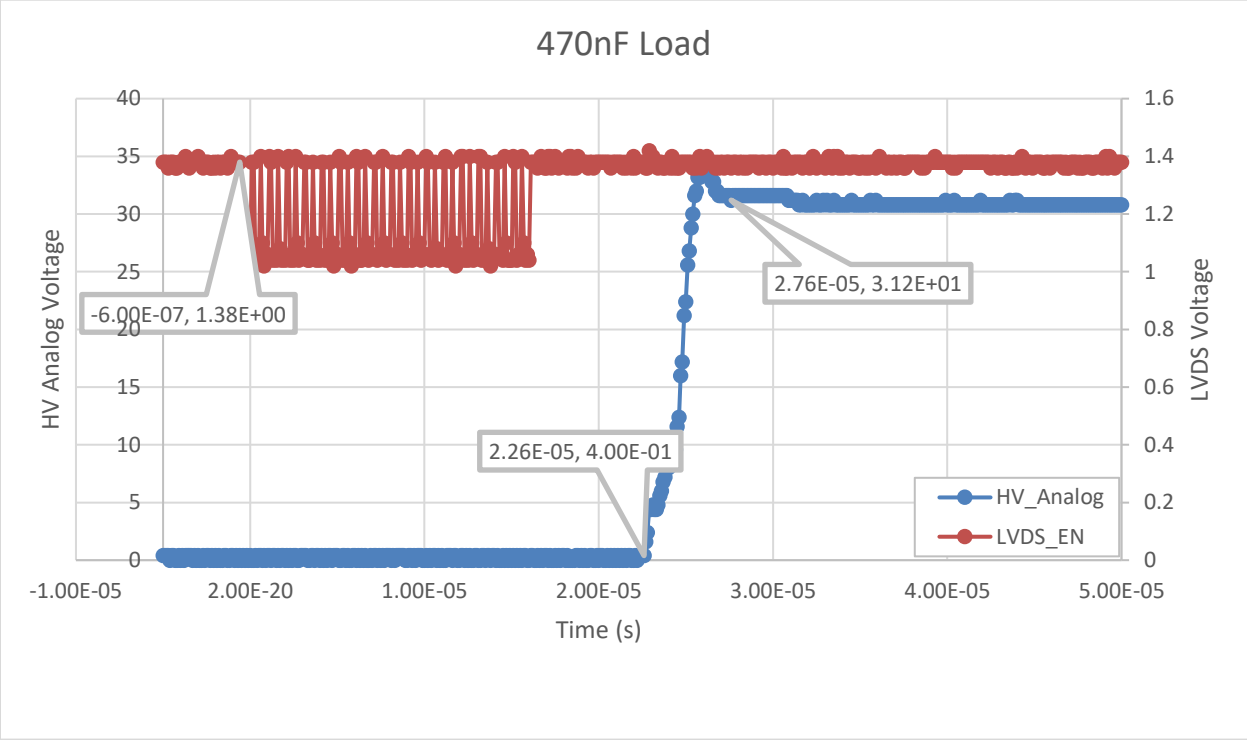
Figure 4: Analog Rise and Fall Times of a 10,000nF Capacitive Load

3 Conclusions

We measured the overall latency of the current generation of 3U rack-mount drive electronics at <28µs. It is important to note that this testing was done without the inter-actuator limiting, which can add a few microseconds to the overall results, but is generally not a significant increase to the system performance.



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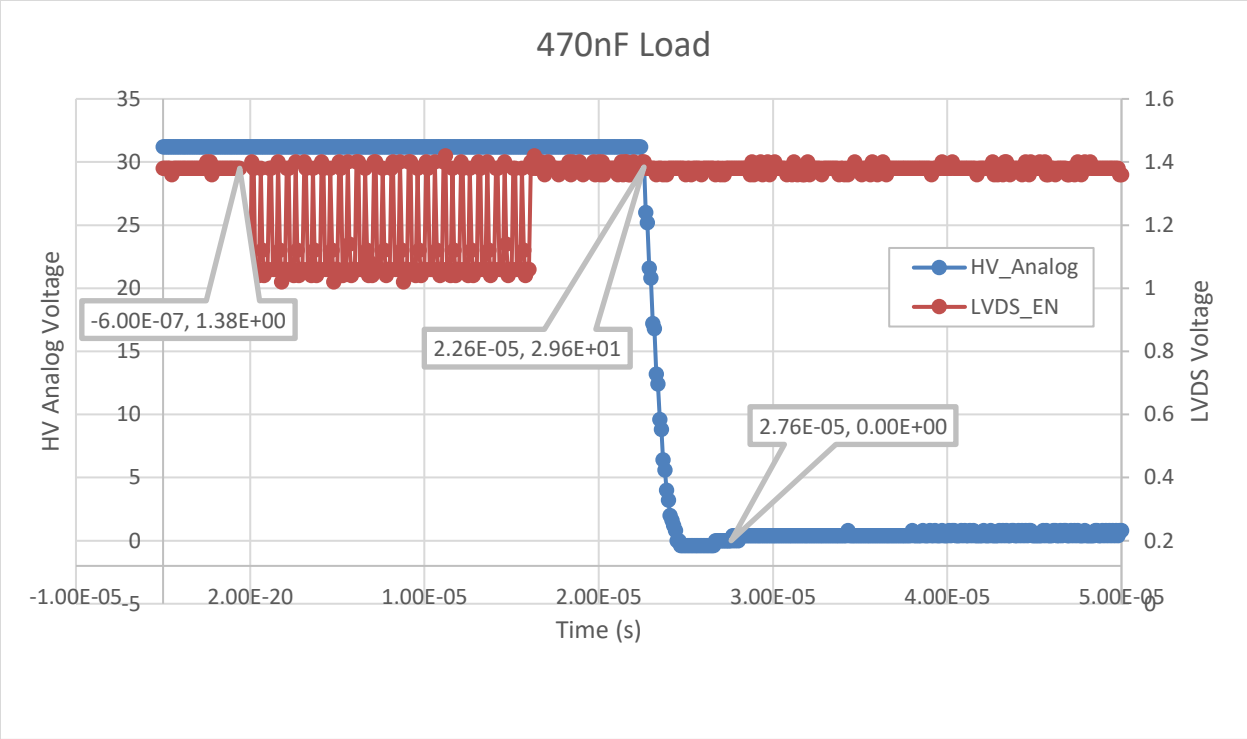

Figure 5: (top) Total System Rise Time Latency; (bottom) Total System Fall Time Latency

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